VT1682 Console and One Bus 8+ 16 Systme

General Description

VT1682 includes the main CPU, Graphic Processor, Sound CPU, internal SRAM (8K bytes for program and 4K bytes for video) ROM (4Kbytes), and some I/O controllers. There are two main systems in VT1682, program system and video system.

Main CPU plays the key role in program system. It can access the internal and external program memories. The program memory stores the program command, instructions, and sound data. VT1682 is equipped with 8K Bytes SRAM as internal program memory. This program RAM will be the zero pages RAM, STACK and some memory of CPU. Program system controls the operations of education machine, including figure, voice, and the title. It means CPU will control the video system to display the specified figure.

Graphic Unit is the main role of the video system. It can access the video memory automatically to display some figures. In addition to the internal program SRAM, VT1682 is equipped the other 4K Bytes SRAM for Video RAM. Internal Video RAM stores pattern vectors for 2 layers of background. External Video memory stores the video characters to be pointed by the pattern vectors.

Sound CPU shared the internal ROM and 4K bytes program SRAM with main CPU. It has the individual IO and ALU. It operates four times faster than main CPU, and suits for different applications

Featuress

System

- Working Voltage 3.0~3.6 V
- Main CPU: 6502 @5.3693MHz in NTSC and 5.3203MHz in PAL
- Internal optional Program ROM: 4K Bytes
- Internal Main CPU Program RAM: 8K Bytes (4K bytes local RAM and 4K bytes shared RAM)
- Internal Video RAM: 4K Bytes
- Direct Memory Access (DMA) Sprite RAM / VRAM / Program RAM / External memory
- Single 16 bits data bus
- Scan line IRQ / 16-bit Timer IRQ / External IRQ
- Expandable memory up to 32M bytes with 3 addresses decoder (CSB).
- T.V. signal output (NTSC, PAL, PAL-M, PAL-N)
- Extend 5 IRQ service entries
- 56 GPIO ports, 40 are for Main CPU, the other 16 are for Sound CPU.

Peripheral

- ADC: 8bits, 5 Times-Division-Multiplex channels with Voice Gain control
- 4 level low voltage detect
- Master/Slave SPI Interface:
- UART Interface
- TFT LCD Interface.
- STN LCD Interface
- IIS Interface
- IIC interface (Master mode)
- CCIR656/601 Interface
- Enhanced ALU, 16 by 16 multiplier and 32 by16 divider

Graphic Processor

- Resolution: TV 256x240 pixels
- 240 sprites in one frame, 16 sprites in one horizontal line
- 2 independent background layers.
- Background character mode: 16/64/256 indexed color mode.
- Background bitmap mode: 16/64/256 indexed color mode or 32768 colors direct color mode
- Sprites are 16 colors.
- Two 256 colored-Color palettes, maximum display indexed color: 512
- Background vertical extension: x1/x1.5/x2
- Background horizontal line individual scrolling: -128~+127
- Sound CPU
- CPU 6502 @21.4772MHz in NTSC and 26.6017MHz in PAL
- 4Kbytes Shared RAM
- 4Kbytes optional Internal ROM
- 16 GPIO ports
- 16 bits Timer x2
- ALU, 16 by 16 multiplier and 32 by 16 divider

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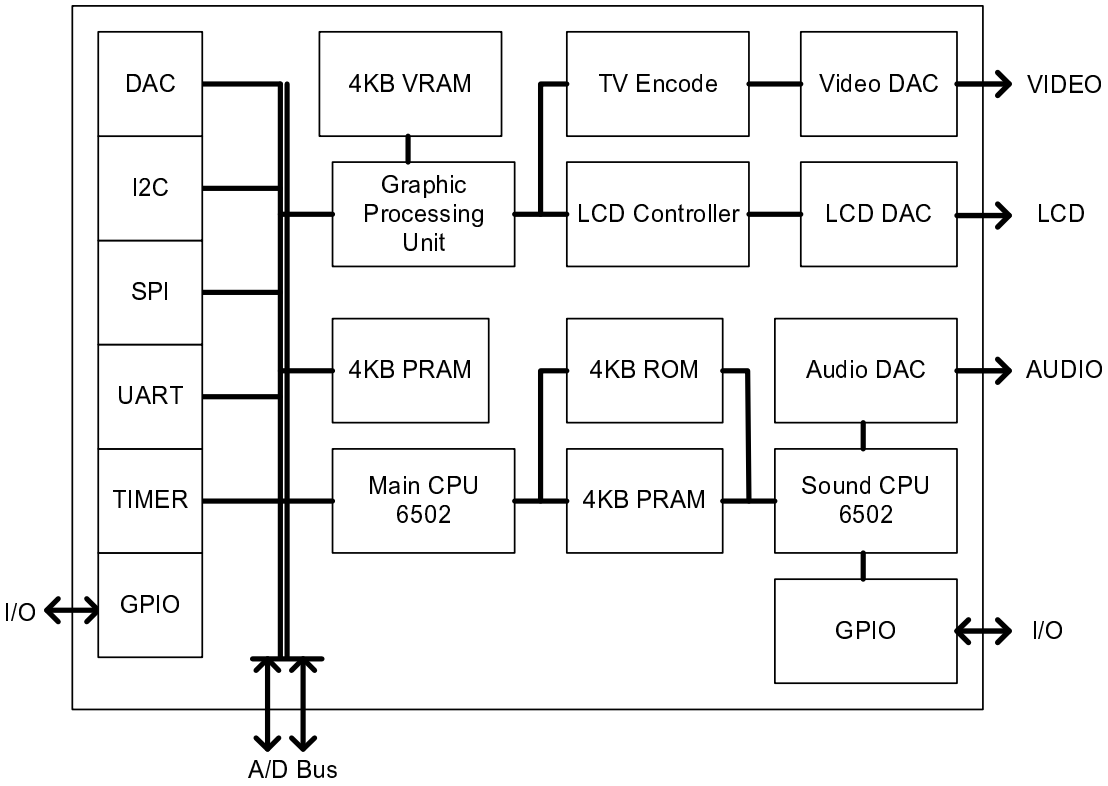
Block Diagram



Absolute Maximum Rating

(Stress in excess of the absolute rating may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability)

DC Supply Voltage: $V_{DD} - V_{SS}$: 0V to 4.5V

Storage Temperature: -50℃ to +125℃

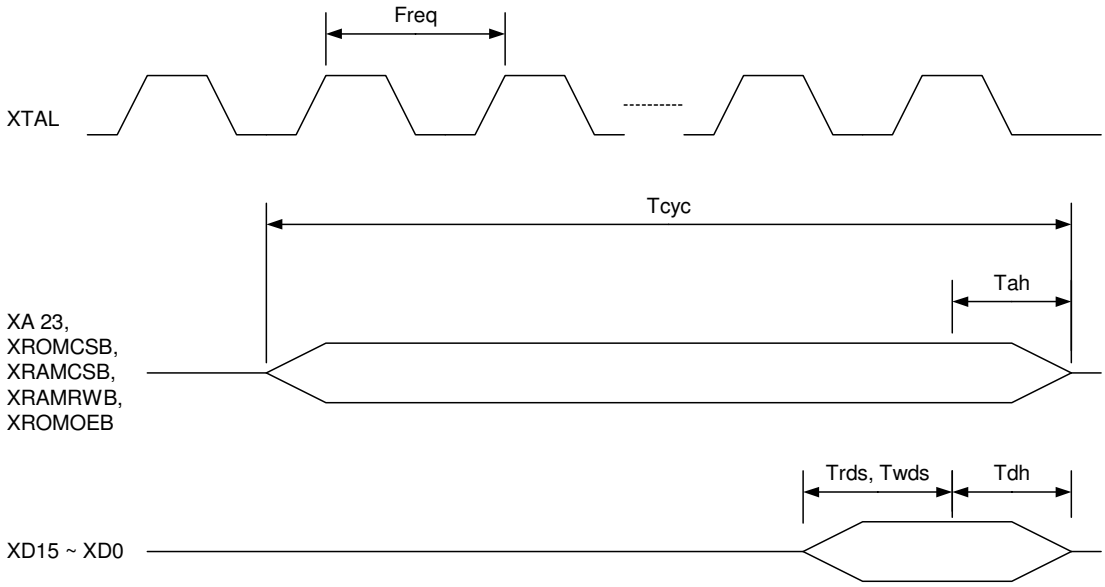
Operating Range

DC Supply Voltage: +3.0V to +3.6V

Operation Temperature:0℃ to +70℃

Electrical Characteristics

AC Characteristics over the operating range



Symbol	Parameter	Min.	Typ.	Max.	Unit
Freq	Frequency of PAL B option		26.601712		MHz
	Frequency of NTSC option		21.47727		MHz
Tcyc	Program cycle time		100/200*		ns
Tdh	Program Data Hold time	10			ns
Trds	Program Read Data Set up time	10			ns
Twds	Program Write Data Set up time	10			ns

* The frequency is decided by the bit D2 of register $2105. The typical of Tcyc is 100ns as D2=1 and 200ns as D2=0.

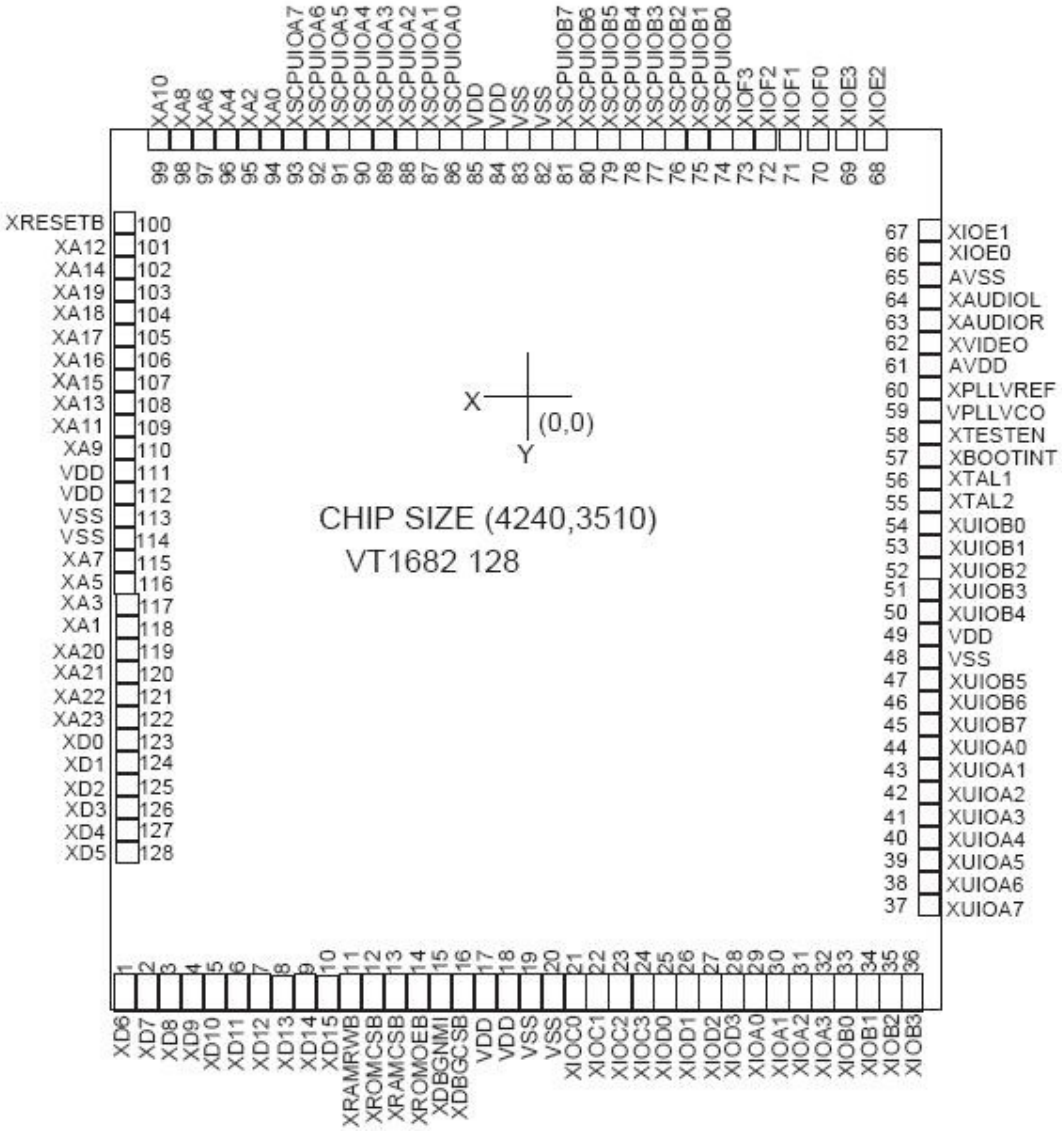
DC Characteristics over the operating range

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIL	Input Low Voltage	-0.5		0.8	V
VIH	Input High Voltage	2.4		VCC+0.4	V
VOL	Output Low Voltage			0.8	V
VOH	Output High Voltage	2.4			V
VCL	Clock Low Voltage	-0.7		0.4	V
VCH	Clock High Voltage	2.5		3.5	V
ICC	Power Supply Current			30	mA
IIL	Input Leakage Current			10	uA
ICL	Clock Leakage			10	uA
ITL	Tri_state Leakage			20	uA
IRL	Reset pin Leakage (pull high R)			1	mA
IOL	Output Low Current	2		10	mA
IOH	Output High Current	2		10	mA

Pin Characteristics over the operating range

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Pull-up Resistor	20	30	50	KΩ
	Pull-down Resistor	20	30	50	KΩ

Pin Configuration



Pin Description

SYMBOL	TYPE	DESCRIPTION
XA[23:0]	O	Address bus
XD[15:0]	I/O	Data bus
XROMCSB	O	1st external memory CSB signal
XRAMCSB	O	2nd external memory CSB signal
XROMOEB	O	External memory OEB signal
XRAMRWB	O	External memory RWB signal
XDEBUGNMI	I	NMI for debug mode
XDEBUGCSB	O	Memory CSB for debug mode
XIOA[3:0]	I/O	Universal I/O
XIOB[3:0]	I/O	Universal I/O
XIOC[3:0]	I/O	Universal I/O
XIOD[3:0]	I/O	Universal I/O
XIOE[3:0]	I/O	Universal I/O
XIOF[3:0]	I/O	Universal I/O
XUIOA[7:0]	I/O	Universal I/O
XUIOB[7:0]	I/O	Universal I/O
XSCPUIOA[7:0]	I/O	Universal I/O
XSCPUIOB[7:0]	I/O	Universal I/O
XTAL1	I	Crystal pin
XTAL2	O	Crystal pin
XBOOTINIT	I	Internal ROM Boot up mode
XPLLVCO	I/O	PLL reference voltage
XPLLVREF	I/O	PLL reference voltage
XVIDEO	O	Composite video signal
XAUDIOR	O	Right channel audio signal
XAUDIOL	O	Left channel audio signal